REMARKS/ARGUMENTS

After entry of this amendment, claims 1-12 and 46-53 will be pending i ı this application. Claim 7 has been amended. Claims 46-53 have been added. Claims 13-4 5 have been cancelled due to a restriction requirement. Support for the new and amended cla ns can be found in the specification, no new matter has been added.

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hatanaka et al (Hatanaka) (United States patent number 5,418,938) in view of Sugita (Jnited States patent number 5,276,842). Claims 2-12 stand rejected under 35 U.S.C. § 103(a as being unpatentable over Hatanaka in view of Sugita in further view of Phelan et al (Phelan) (Jnited States patent number 6,499,089). Reconsideration of these rejections and allowance o the pending claims in light of these amendments and remarks is respectfully requested.

Drawings

The drawings have been objected to. Formal drawings have been filed eparately via express mail.

Claim 1

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hatanaka in view of Sugita. Specifically, the pending office action states that it would be obvious to "have an arbiter that arbitrates access to the memory as taught by Sugita in he invention of Hatanaka et al since this would have helped avoid access conflicts to an a ldress location thus preventing wrong data from being stored or retrieved." (See pending off ce action, page 3, fifth paragraph.)

But these access conflicts do not occur in the circuit described in Hatan ıka, therefore, there is no motivation to combine the arbiter of Sugita in the circuit of Hata aka.

Hatanaka describes a circuit having two CPUs 100 and 200 that share d ıta using a two port memory 300. (See Hatanaka, Figure 3.) Data held by each CPU in respectiv hold circuits 15 and 16 should be identical. (See Hatanaka, column 2, lines 53-54.) Data m odified by CPU 100 is synchronized with CPU 200 by being provided to CPU 200 via transmit c cuit 11,

DPRAM 300, and receive circuit 14. A reverse path from CPU 200 to CPU 100 is sir larly provided. (See Hatanaka, Figure 3.)

These data transfers between the two CPUs 100 and 200 are controlled ›y flags that are set by the CPUs in flag areas 19 and 20. Specifically, a flag set in area 20 mea ıs that data should be transferred, and flags in area 19 control the communications procedure. (See Hatanaka, Figure 3 and column 4, lines 40-43.)

Accordingly, there is no need for an arbitrator in Hatanaka to avoid acc ss conflicts. When one CPU wants to update the other, it provides data and correspondin ; flags to the DPRAM 300. When the receiving CPU sees a flag, it can retrieve the data and upc ate its holding circuit. There appears to be no condition in the circuit of Hatanaka where eac CPU can try to access the same memory location, so there are no potential access conflicts to av ›id, and thus no need for an arbiter.

Also, the combination of cited references does not teach each and every element of this claim. For example, claim 1 recites a "programmable logic integrated circuit co mprising: a programmable logic portion; and...a processor; and a memory block." The combina ion of cited references does not provide this feature.

The pending office action cites Figure 3 and column 3, lines 33 and 36 of Hatanaka as disclosing this. (See pending office action, page 2, paragraph 3a.) Specil cally, the EEPROM 500 of Hatanaka is equated with the recited programmable logic portion, th CPU 100 is equated with the recited processor, while the DPRAM 300 is equated with the recite l memory block . (See pending office action, page 2, paragraph 3a.)

But Figure 3 of Hatanaka shows an EEPROM 500 separate and apart fr ›m the CPU 100. It does not appear that the EEPROM 500 is included on an integrated circu . with the CPU 100. In fact, the boundaries of the EEPROM 500 and CPU 100 suggest that they are on separate integrated circuits, not on an integrated circuit as required by the claim. Simi arly, Figure 3 of Hatanaka shows an DPRAM 300 separate and apart from the CPU 100. D 'RAM 300 does not appear to be included on an integrated circuit with the CPU 100, again th :

boundaries of the DPRAM 300 and CPU 100 suggest that they are on separate integrat :d circuits.

For at least these reasons, claim 1 should be allowed.

Claim 3

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hatanaka in view of Sugita in further view of Phelan. But these references do not sho / or suggest each and every element of this claim. For example, claim recites: "wherein th programmable logic portion comprises a plurality of logic elements, programmably co ıfigurable to implement user-defined combinatorial or registered logic functions." These referen es do not provide this feature.

The pending office action cites column 3, line 36 of Hatanaka as showi .g this. Specifically, the pending office action states that the EEPROM 500 of Figure 3 reads (n the recited programmable logic portion. (See pending office action, page 4, paragraph b.)

But an EEPROM is simply a memory device. (See, for example, IEEE "Comprehensive Dictionary of Electrical Engineering," IEEE press, 1999. A memory levice stores data for retrieval. It does not implement user-defined combinatorial or registere l logic functions as required by the claim.

For at least these reasons, claim 3 should be allowed.

Claim 7

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hatanaka in view of Sugita in further view of Phelan. But again, it is not obvious to c mbine the arbiter of Sugita with the circuit of Hatanaka. For example, there is no motivation to (ɔmbine the arbiter of Sugita with the circuit of Hatanaka because Hatanaka uses a flag scheme to transfer data between two CPUs such that an arbiter is not needed.

Also, the combination of references do not teach each of the claimed el ments on an integrated circuit, as discussed above. Further, as discussed above, the EEPROM 5)0 of Hatanaka is not programmable logic "configurable to implement user-defined combin torial or registered logic functions" as required by the claim.

Moreover, these references do not show or suggest each and every elem ent of this claim. For example, claim 7, as amended, recites: "when the second port is accessing subset of the first plurality of memory cells, the arbiter prevents the first port from accessing the first plurality of memory cells, and when the second port is accessing the subset of the first plurality of memory cells, the arbiter allows the first port to access the second plurality of mem ry cells." These references do not provide this feature.

The pending office action cites Sugita, column 2, lines 38-40 and colun n 4, lines 8-21 as showing this. (See pending office action, page 8, last paragraph.) But these ci ed passages teach an arbitration scheme where a busy signal is sent to a port "B" that is tr ing to read the same memory cell as port "A" is writing to.

This is different than preventing access to a first plurality of memory ce ls when only a subset is being accessed. In Sugita, apparently only the cell being read by one p ort is blocked from access by the second port. In the claim as recited, access to all the first p lurality of memory cells is blocked.

For at least these reasons, claim 7 should be allowed.

Other Claims

The other claims depend on the above claims, and should be allowed fc at least the same reasons, and for the additional limitations they recite. The new claims 46-53 should be allowed for at least similar reasons.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in his application are in condition for allowance. The issuance of a formal notice of allowan e at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosec tion of this application, please telephone the undersigned at 415-273-4782.

Respectfully submitted,

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